Signal Integrity Design of TSV and Interposer in 3D-IC

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***Abstract*—Electrical characterization of through-silicon via (TSV) and interposer line becomes more important as 3-dimensional integrated circuit (3D-IC) is emerging. In this paper, TSV modeling is proposed and verified using 3D-EM simulation. The model has good correlation with the simulation both at insertion loss and TSV-to-TSV noise transfer function. Using the TSV model, signal integrity (SI) analysis is performed. Also, interposer line characteristics are analyzed both at frequency- and time- domain. As a result, SI can be considered based on the TSV and interposer line analyses for 3D IC design.**

Keywords—noise coupling; interposer; modeling; thorugh-silicon via (TSV);

I. INTRODUCTION

According to Moore's law, the number of transistors on a chip doubles in every 18 months and the transistor-size shrink leads to achieve the law until now. However, it encounters several limitations because of the lithography difficulty, high power consumption, unstable interconnection, and so on [1]. As an alternative solution to increase transistor density in limited area, 3-dimensional integrated circuits (3D-ICs) are emerging these days. In 3D-IC, through-silicon via (TSV) is the key item for the interconnection between vertically stacked dies. TSV-based 3D-IC has several advantages compared with conventional 2D-IC except the increased transistor planar density. Because TSV length is very short and could be located in any place of a die, more high frequency signal could be transferred using the increased number of TSV I/Os; it dramatically increases bandwidth between stacked dies compared with 2D-IC [2]. For the efficient placement of 3D-stacked chips, interposer is also emerging recently. Using the fine-pitch planar routing, the bandwidth could increases compared 2D system.

To maximize the advantages of TSV and interposer, electrical characteristic of TSV and interposer line should be analyzed well. TSVs are formed on the conductive silicon substrate and insulation layer between TSV and silicon is necessary; it blocks leakages through silicon substrate. However, TSV insulation layer is usually very thin due to the manufacturing time and high capacitance exists between TSV and silicon substrate. So, the isolation effect decreases as frequency increases. It generates high loss and high noise coupling through silicon substrate at high frequency. Similar problem occurs at interposer line.

In previous works, several TSV and line modeling methods are proposed and electrical characteristics of TSV channel are also analyzed [3-5]. Still it has limitations that noise coupling and propagations are not analyzed at the same time. In practical 3D-IC, a lot of TSV and lines are located in the small area and noise coupling and signal propagation should be considered at the same time. In Fig. 1, lots of TSVs are placed in the limited area and the received signal eye-diagram quality is degraded depending on the TSV signal propagation characteristics. At the same time, the adjacent TSV channel is affected by the coupling signal.

In this paper, TSV electrical modeling is proposed and both noise coupling and signal propagation characteristics are considered at the same time. Also, interposer line characteristics are analyzed. Considering both TSV and interposer line, signal propagation and noise coupling analysis is performed, which leads to optimal design concerning signal integrity (SI) characteristics.

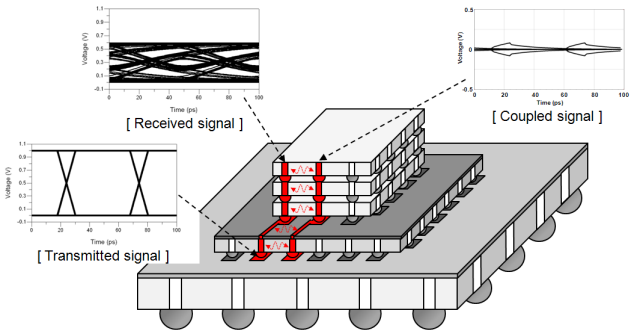

Fig. 1. A conceptual figure of 3D-IC system with vertically stacked chips using TSVs. Due to the lossy silicon substrate, signal is degraded at the receiver. Also signal is coupled to the adjacent channel, which generates noise and degrades circuit performance

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II. MODELING AND ANALYSIS OF TSV CHANNEL

To model TSV signal propagation and TSV-to-TSV noise coupling at the same time, we used 3-dimensional transmission line methods (3D-TLM). In 3D-TLM, whole structures are divided into several repeating unit cells and each unit cell is modeled as lumped R, L, G, C. Then, by combining each unit cells, whole structure modeling could be done. For TSV modeling, TSV and silicon substrate unit cell modeling is necessary and the model is illustrated in Fig. 2.

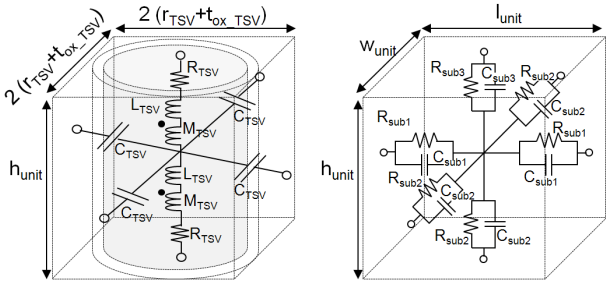


Fig. 2. Equivalent circuit model of 3D-TLM unit cells: (a) TSV unit cell (b) silicon substrate unit cell

TSV unit cell is constructed by series resistance, inductance, and parallel capacitance. The silicon substrate unit cell model is constructed by parallel resistance and capacitance. Each value could be obtained using the following equations [5].

$$C_{TSV} = \frac{1}{4}\frac{2\pi \cdot \varepsilon_{ox\_TSV} \cdot h_{unit}}{\ln\left(\frac{r_{TSV} + t_{ox\_TSV}}{r_{TSV}}\right)} \quad (1)$$

$$L_{TSV} = \frac{1}{2}\frac{\mu \cdot h_{TSV}}{2\pi} L(r_{TSV})\frac{h_{unit}}{h_{TSV}} \quad (2a)$$

$$M_{TSV} = \frac{1}{2}\frac{\mu \cdot h_{TSV}}{2\pi} L(p_{TSV})\frac{h_{unit}}{h_{TSV}} \quad (2b)$$

Where

$$L(x) = ln\left(\left(\frac{h_{TSV}}{x}\right) + \sqrt{\left(\frac{h_{TSV}}{x}\right)^2 + 1}\right) + \frac{x}{h_{TSV}} - \sqrt{\left(\frac{x}{h_{TSV}}\right)^2 + 1}$$

$$R_{sub1} = \frac{1}{2}\frac{1}{\sigma}\frac{l_{unit}}{w_{unit}h_{unit}} \quad (3a) \qquad C_{sub1} = 2\varepsilon_{silicon}\frac{w_{unit}h_{unit}}{l_{unit}} \quad (3b)$$

For the verification of TSV modeling using 3D-TLM, the results are compared with the 3D-EM simulator results. We used Ansys HFSS for the verification. The target structure has four TSVs and four port. Two TSVs are signal TSV and the other two TSVs are ground TSV and are connected each other for the reference. The simulated structure and the results are illustrated in Fig. 3. Here, TSV diameter is 30um pitch between TSVs are 100 um, TSV insulation layer thickness is 0.5 um, and TSV height is 100 um. The modeled and simulated results have very good correlation up to 20GHz both at insertion loss and noise transfer function.

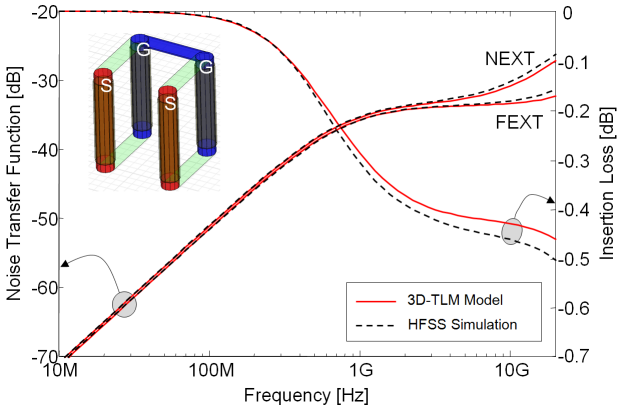


Fig. 3. Modeld and 3D-EM simulated results of TSV noise transfer function and insertion loss. Target TSV structure has two signal TSV and two ground TSV. The results show that the model and simulation has very good correlation up to 20 GHz.

To obtain good SI, we need to decrease TSV-to-TSV noise coupling while also decreasing TSV insertion loss. As a parameter for SI, eye-diagram is usually used. So, time-domain simulation is performed using the modeled coupled TSV structure. In time-domain simulation, we considered 50 Ω input resistance and 10 fF output capacitance for the termination. The results are illustrated in Fig. 4.

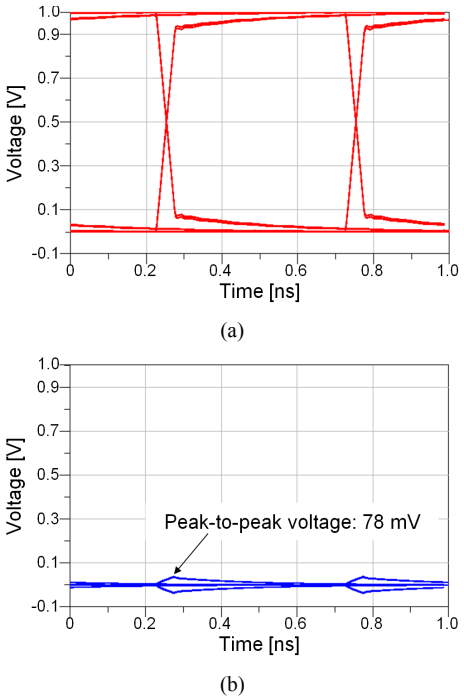


Fig. 4. (a) Eye-diagrams of the coupled TSV channel (b) Eye-diagram of the adjacent silent TSV channel when 0-1 V, 50 ps risign/falling time 2Gbps signal is inserted into coupled TSV channel

In Fig. 4, eye-diagram of the transmitted and coupled signal is illustrated for TSV channel in Fig. 3. Because the insertion loss is only about -0.5 dB up to 20 GHz, the eye-diagram shows good quality. TSV-to-TSV noise coupling could be more important than TSV insertion loss for TSV structures. Depending on the TSV noise coupling voltage, TSV channel receiver eye-diagram height could be changed about 80 mV in this case.

III. Analysis of Interposer Line Channel

For interposer design considering SI, on-interposer line could be more critical than TSV because of its longer length. At interposer, line length increases much longer than the conventional on-chip lines: both insertion loss and noise coupling could be a big problem. Coplanar-type coupled lines on silicon interposer could be modeled as illustrated in Fig. 5.

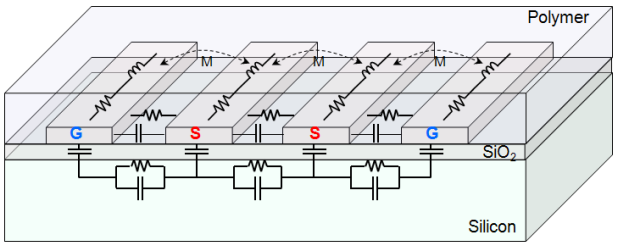


Fig.5 Simplified circuit model of coupled lines on silicon interposer

In Fig.5, metal lines are located very close to lossy silicon and large capacitance exists between metal and silicon like the case of TSV. Generally, simplified model of on-silicon metal line could be constructed as oxide capacitance, C_{ox}, and parallel silicon capacitance and conductance, C_{si} and G_{si} as illustrated in Fig. 6.

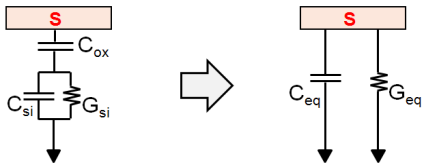


Fig.6 Simplified circuit model of on-siliocn metal line and its equivalent capacitance and conductance. The equivalent C and G varies depending on frequency.

In Fig. 6, the equivalent capacitance and conductance could be calculated using the following equations.

$$C_{eq} = \frac{C_{ox}\left(G_{si}^{\ 2} + C_{si}\cdot\omega^2(C_{Si}+C_{ox})\right)}{G_{Si}^{\ 2} + \omega^2(C_{Si}+C_{ox})^2} \quad (4)$$

$$G_{eq} = \frac{G_{Si}\cdot C_{ox}^{\ 2}\cdot\omega^2}{G_{Si}^{\ 2} + \omega^2(C_{Si}+C_{ox})^2} \quad (5)$$

At low frequency, C_{eq} is equal to C_{ox} while it is equal to C_{si} at high frequency. For conductance, G_{eq} is 0 at low frequency and G_{eq} becomes have the same value as G_{si} at high frequency.

For the coplanar-type coupled on-interposer lines as illustrate in Fig. 5, capacitance and conductance are extracted from the simulated s-parameter. For the simulated coupled lines, the width and space of metal line is 25 um, and thickness is 3 um. The distance between metal and silicon is 1 um for M1-layer routing and 8 um for M3-layer routing. The extracted capacitance and conductance per unit length is shown in Fig. 7.

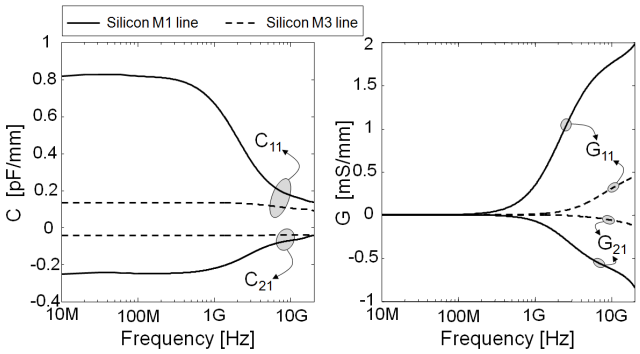
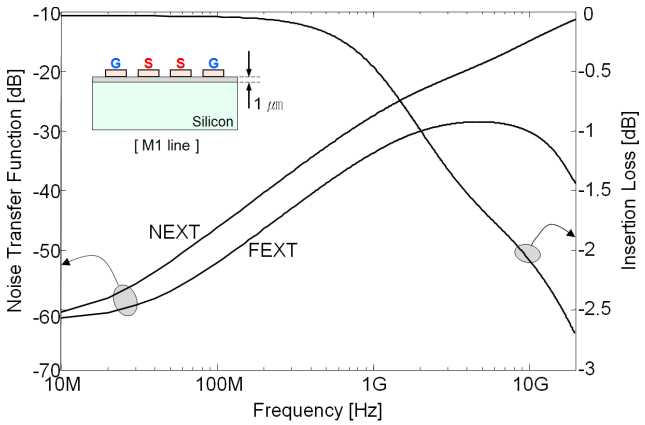


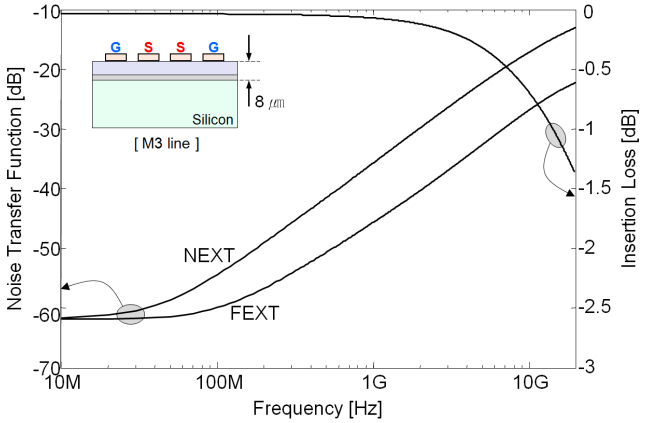
Fig.7 Extracted capacitance and conductance from the simulated on-interposer coupled lines. Both self and mutual terms are illustrated. The values are frequency-dependent as we expected.

In Fig. 7, both self and mutual terms are illustrated and capacitance and conductance is a function of frequency as we expected using the Eq. 4 and Eq. 5. For M1 routing, both C and G change a lot depending on frequency while it has small change for M3 routing. Because of large C_{ox} for M1 routing, it is expected that both insertion loss and noise coupling is mainly affected by this frequency-dependent capacitance. For the same structure with 1000 um length, the simulated noise transfer function and insertion loss are illustrated in Fig. 8.

The insertion loss of on-interpose line is much severe than TSV channel because of its long length. The self capacitance, C_{11}, is the dominant loss mechanism for both M1 and M3 routing case. For the noise coupling, capacitive and inductive coupling occurs at the same time. However, mutual capacitance, C_{21}, is very large for M1 routing and capacitive coupling is dominant for M1 routing while inductive coupling is more superior than capacitive coupling at M3 routing. As a result, M1 routing shows much noise coupling than M3 routing for near-end cross talk (NEXT). NEXT increases as frequency increase for both M1 and M3 routings. However, far-end cross talk (FEXT) does not increase as frequency increases for M1 routing and FEXT for M3 is larger than M1 case at high frequency over 10 GHz. As frequency increases, insertion loss increases and the coupled signal also experience large loss. For FEXT, the coupled waveform should propagate to the end of the line experiencing the high loss. Therefore, FEXT decreases as frequency increases at high frequency. For M3 routing, insertion loss is smaller than M1 routing and FEXT also increases as frequency increase up to 20 GHz.



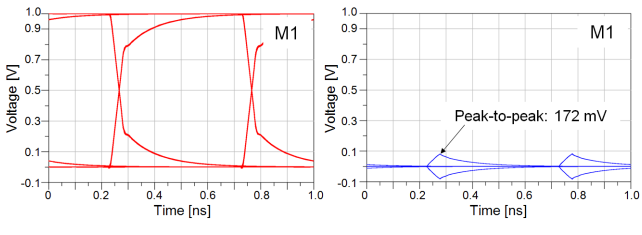
(a)



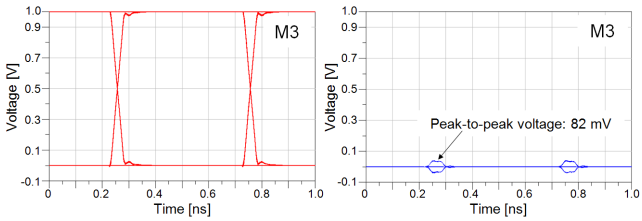
(b)

Fig.8 Noise transfer function and insertion loss of the coplanar-type coupled lines on silion interpsoer. Metal width is 25 um, space is 25 um, and thickness is 3 um: (a) line is on M1 layer, where distance between metal and silicon substrate is 1 um. (b) line is on M3 layer, where distance between metal and silicon substrate is 8 um.

For more clear understanding of on-interposer coupled line characteristics, time-domain simulation is performed and the eye-diagram is plotted in Fig. 9. The termination and input voltage are same as TSV case: Input voltage is 2 Gbps 0-1V PRBS with rising/falling time of 50 ps, the input resistance is 50 Ω, and the output capacitance is 10 fF. The eye-diagrams of the interposer lines are worse than that of TSV channel for M1 routing, but is better for M3 routing because the M3 coupled line insertion loss under several GHz is better than TSV channel. Concerning the noise coupling, M1 line shows much larger coupled voltage while the M3 line has similar coupled voltage compared with TSV case. For TSV and M1 line, noise coupling is mainly due to the capacitance through the silicon substrate while the M3 is partly due to the capacitance and partly due to the mutual inductance. Because this capacitive coupling through silicon substrate is much larger for TSV, it shows similar coupling voltage even though the length is 10 times smaller than M3 coupled line.



(a)



(b)

Fig.9 Eye-diagrams of the interposer at the receiver and adjacent silent line when 0-1 V, 50 ps risign/falling time 2Gbps signal is inserted. The line length is 1000 um and (a) coupled lines are on M1 (b)coupled lines are on M3

IV. CONCLUSIONS

As 3D-IC emerges in the industry, precise analysis of TSV and interposer line becomes important for system design considering SI. Both insertion loss and noise coupling are important factors to guarantee SI. Thus, they are analyzed for the TSV and the interposer line. For the TSV, the noise coupling is the more considerable factor than the insertion loss. A TSV-to-TSV noise coupling is about -35 dB at 1GHz for the TSV diameter of 30 um and the height of 100 um. For the interposer line, the routing layer is critical to both the insertion loss and the noise coupling. If the metal line is closely located to the silicon substrate such as M1 metal layer, large SiO_2 capacitance affects to both characteristics. However, if the metal line is placed farther from the silicon substrate, the insertion loss and the noise coupling decrease. If the metal line is 8 um far from the silicon substrate in case of M3, the eye-diagram at 2 GHz has better quality than the TSV. And the noise coupling voltage is similar with that of the TSV even though the metal line (M3) length is 10 times longer than the TSV.

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